Abstract

Embodiments of the present invention relate to high-performance processors, and more specifically, to processors that store all operation information associated with each instruction in a single memory. A processor including multiple programmable logic arrays (PLAs); an instruction pointer queue coupled to the multiple PLAs; and an instruction pointer sequencing logic/predictor component coupled to the instruction pointer queue. The processor further includes a micro-operation cache coupled to the instruction pointer sequencing logic/predictor component; a micro-operation memory coupled to the micro-operation cache; and a trace pipe (TPIPE) coupled to the micro-operation cache and the instruction pointer queue.

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